Listing of Claims

Claim 1 (currently amended). A system for tracing information for a plurality of instructions having an instruction order, comprising:

a trace data bus; and

a trace data order determination element configured to generate a trace data order signal when trace data becomes available for a cache miss, said trace data order signal specifying ~~a trace data transfer order that is different from said instruction order, wherein said trace data order signal specifies a transfer order relative to~~ how the trace data may be mapped to a current ranking of the relative age of previously executed instructions having outstanding trace data;

wherein said trace data order signal is transmitted with said trace data such that trace data for the cache miss may be matched to a corresponding instruction generating the cache miss.

Claim 2 (original). The system of claim 1, wherein said trace data order signal is transferred on said trace data bus.

Claim 3 (previously presented). The system of claim 1, wherein said trace data order signal identifies a number of instructions that have outstanding trace data.

Claim 4 (original). The system of claim 1, wherein said trace data is load data.

Claim 5 (previously presented). The system of claim 4, wherein a load address for said load data is received prior to receiving said load data from memory and said load address is transferred on said trace data bus prior to receipt of said load data from memory.

Claim 6 (original). The system of claim 4, wherein said load data is transferred on said trace data bus with a load address if said load data is immediately available.

Claim 7 (currently amended). A computer program product for use in a system for tracing information for a plurality of instructions having an instruction order, comprising:

computer-readable program code for causing a computer to describe a trace data bus;

computer-readable program code for causing a computer to describe a trace data order determination element configured to generate a trace data order signal when trace data becomes available for a cache miss, said trace data order signal specifying ~~a trace data transfer order that is different from said instruction order, wherein said trace data order signal specifies a transfer order relative to~~ how the trace data may be mapped to a current ranking of the relative age of previously executed instructions having outstanding trace data; and

a computer-usable medium configured to store the computer-readable program codes;

wherein trace data for a cache miss is traced when it becomes available and said trace data order signal is transmitted with said trace data for said cache miss to indicate which previously traced instruction generated the trace data.

Claim 8 (currently amended). A method for enabling a computer to generate a system for transferring trace information for a plurality of instructions having an instruction order, comprising:

transmitting computer-readable program code to a computer, said computer-readable program code including:

computer-readable program code for causing a computer to describe a trace data bus; and

computer-readable program code for causing a computer to describe a trace data order determination element configured to generate a trace data order signal when trace data becomes available for a cache miss, said trace data order signal specifying ~~a trace data transfer order for trace data generated by said plurality of instructions that is different from said instruction order, wherein said trace data order signal specifies a transfer order relative to~~ how the trace data may be mapped to a current ranking of the relative age of previously executed instructions having outstanding trace data;

wherein trace data for a cache miss is traced when it becomes available and said trace data order signal is transmitted with said trace data for said cache miss to indicate which previously traced instruction generated the trace data.

Claim 9 (original). The method of claim 8, wherein computer-readable program code is transmitted to said computer over the Internet.

Claim 10 (currently amended). A computer data signal embodied in a transmission medium, comprising:

computer-readable program code for causing a computer to describe a trace data, said trace data being associated with a plurality of instructions having an instruction order; and

computer-readable program code for causing a computer to describe a trace data order determination element configured to generate a trace data order signal when trace data becomes available for a cache miss, said trace data order signal specifying ~~a trace data transfer order that is different from said instruction order, wherein said trace data order signal specifies a transfer order relative to~~ how the trace data may be mapped to a current ranking of the relative age of previously executed instructions having outstanding trace data;

wherein trace data for a cache miss is traced when it becomes available and said trace data order signal is transmitted with said trace data for said cache miss to indicate which previously traced instruction generated the trace data.

Claim 11 (currently amended). A method for transferring trace data, comprising:

transferring trace data for a plurality of instructions in an order different from a program sequence of said plurality of instructions, and

transmitting a trace data order signal with said trace data wherein a transfer of trace data for a particular instruction is specified relative to at least one instruction having outstanding trace data by said trace data order signal, said trace data order signal specifying how the trace data may be mapped to a current ranking of the relative age of previously executed instructions having outstanding trace data;

wherein trace data for a cache miss is traced when it becomes available and said trace data order signal is transmitted with said trace data for said cache miss to indicate which previously traced instruction generated the trace data.

Claim 12 (original). The method of claim 11, wherein said transfer of trace data for said particular instruction is specified relative to one outstanding instruction.

Claim 13 (currently amended). The method of claim 12, wherein said ~~transfer of trace data for said particular instruction is accompanied by a~~ trace data order signal ~~that~~ indicates that trace data for said one outstanding instruction is still outstanding.

Claim 14 (original). The method of claim 11, wherein said transfer of trace data for said particular instruction is specified relative to a plurality of outstanding instructions.

Claim 15 (currently amended). The method of claim 14, wherein said trace data order ~~transfer of trace data for said particular instruction is accompanied by a~~ signal ~~that~~ indicates that trace data for said plurality of outstanding instructions is still outstanding.

Claim 16 (previously presented). The method of claim 15, wherein said signal indicates a number of instructions that have outstanding trace data.

Claim 17 (original). The method of claim 11, wherein said trace data is load data.

Claim 18 (previously presented). The method of claim 17, wherein a load address for said load data is received prior to receiving said load data from memory and said load address is transferred on said trace data bus prior to receipt of said load data from memory.

Claim 19 (original). The method of claim 17, wherein said load data is transferred on said trace data bus with a load address if said load data is immediately available.

Claim 20 (currently amended). A method for transferring trace data, comprising:

tracing a plurality of instructions having an instruction order;

transferring trace data for instructions in said plurality of instructions when said trace data becomes available, wherein said transfer order is different from said instruction order; and

transmitting a signal along with said transferred trace data that ~~identifies a number of instructions that have trace data outstanding order, wherein said signal specifies a transfer order relative to~~ specifies how the trace data may be mapped to a current ranking of the relative age of previously executed instructions having outstanding trace data;

wherein trace data for a cache miss is traced when it becomes available and said signal transmitted along with said transferred trace data indicates which previously traced instruction generated the trace data.

Claim 21 (original). The method of claim 20, wherein said trace data is load data, and said transmitted signal identifies a number of instructions that have load data outstanding.

Claim 22 (original). The method of claim 21, wherein a load address for said load data is transferred on said trace data bus prior to receipt of said load data from memory.

Claim 23 (original). The method of claim 21, wherein said load data is transferred on said trace data bus with a load address if said load data is immediately available.